UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,370	05/20/2004	Naoki Yazawa	042387	6253

38834 7590 08/28/2007

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
SIM, YONG H	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
08/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/849,370	YAZAWA, NAOKI	
	Examiner	Art Unit	
	Yong Sim	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/18/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 4, 6, 8, 10, 12, 14, 18 - 19 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 4, 6, 8, 10, 12, 14, 18 - 19 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 21 objected to because of the following informalities: change the word "form" to "from" in line 3. Appropriate correction is required.

Response to Arguments

1. Applicant's arguments filed 6/18/20007 have been fully considered but they are not persuasive.

Applicant's representative argues on pg. 10 that the invention is characterized in that the current from the reverse bias voltage is used in the light emission drive during and after the starting time of a light emission drive.

Examiner agrees with Applicant that the specification describes the invention as described in Applicant's argument.

However, the claims do not recite exactly as Applicant argues. For example, claim 1 merely recites in lines 15 – 17, "parasitic capicitances of light emitting elements in the non-scan state is supplied as a forward current to a light emitting element," which Yoshida accurately describes in Fig. 9. In figure 9c, parasitic capacitances of light emitting elements in the non-scan state is supplied as a forward current to a light emitting element (E12). In the next stage show in Fig. 9d, the light emitting element is scanned and lit.

Therefore, the argument is moot.

Re claim 1, Applicant argues that Yoshida fails to disclose a structure of "a gradation control means which can change repeating times of scans within a unit time," in lines 4 – 5 on page 10.

However, Examiner respectfully disagrees since Yoshida teaches changing the repeating times (increasing the pulse generation by increasing the drive period as explained in Para 0078) of scans to extend the light emission time of EL elements to increase brightness within one unit of time which is one frame (Para 0073 – 0075).

Therefore, the argument is moot.

2. Applicant's arguments with respect to claim 1 has been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1 – 4, 18 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida et al. (Hereinafter "Yoshida" US 2003/0052842 A1).**

Re claim 1, Yoshida teaches a drive device of a light emitting display panel (1 "display panel" Fig. 1) provided with a plurality of data lines (A1 – An "anode/drive lines" Fig. 1) and a plurality of scan lines (B1 – Bm "cathode/scan lines" Fig. 1) which intersect one another and capacitive light emitting elements (E11 – Enm "Organic EL elements" Fig. 1) having a diode characteristic which are respectively connected at intersecting positions between the respective data lines and the respective scan lines [See Fig. 2 and Para 0060], comprising;

a scan driver (3 "cathode line scan circuit" Fig. 1) which performs scan one after another by connecting the respective scan lines to a scan potential point as well as connecting a scan line of a non-scan state which is not connected to the scan potential point to a driving voltage source (See Fig. 9; In 9A, when B1 is scanned, the scan line is connected to a scan potential, and non-scanning lines are connected to a Vm, a voltage source [Para 0019 - 0020].) and a data driver which controls lighting or non-lighting of the respective light emitting elements of a scan state in synchronization with a scan of the scan driver (Para 0067; "output processing circuit supplies a drive control signal in accordance with the pixel data supplied to the anode line drive circuit in synchronism with the (scan) timing signal.), wherein

by being constructed in such a way that the scan driver and the data driver set all scan lines and all data lines at a same electrical potential when a scan is switched so that electrical charges accumulated in parasitic capacitances of the respective light emitting elements are discharged (Para 0019; "the anode drive line and all cathode scan lines are reset to the ground potential, so that all electric charge is discharged.")

and that charge current which follows the discharge of electrical charges, which is from the driving voltage source, and which charges parasitic capacitances of light emitting elements in the non-scan state (Para 0020; "charging is performed by a voltage as shown by arrows for the parasitic capacitance of elements/(non-scanning elements) other than the element that emits light.") is supplied as a forward current to a light emitting element which is scanned and lit, the light emitting element is driven to emit light, utilizing the driving voltage source (As shown by figure 9, the light emitting element E12 is driven by applying the current from the non-scanning elements by utilizing a voltage source Vm along with current source I1 [Para 0020].), wherein

the drive device further comprises a gradation control means which can change repeating times of scans within a unit time (Para 0038; "light-emitting elements in the luminescence display panel are repeated scanned to control light emission/gradation." Fig. 5 shows the change of repeating times of scans. Although, Fig. 5 shows the increase in one line period, over all the changes occur in a unit time of one frame. See Para 0073.) and wherein the gradation control means controls changing of the repeating times of scans so that the more the number of repeating times of scans during the unit time, the higher the entire intensity level becomes, and the less the number of repeating times of scans, the lower the entire intensity level becomes (Para 0083; "in a passive matrix display device of this embodiment, when the partial display is selected and the one line period is increased, the light emission time of the display elements is increased/(As can bee seen in Fig. 5, the increase in one line period increases the number of repeating times of scans), thereby the luminance of a display screen is

substantially increased. In addition to the above, since the control is performed so that the ratio of the drive period is increased in the one line period in this embodiment, the luminance of the display screen is substantially further increased.").

Re claim 2, Yoshida teaches the drive device of the light emitting display panel according to claim 1, characterized by being constructed in such a way that the scan driver and the data driver connect all scan lines and all data lines to the scan potential point, respectively, when a scan is switched so that the scan lines and the data lines are set at a same electrical potential (See Fig. 9B; All Scan and drive lines are connected to ground (electrical potential) when a scan is switch from B1 to B2. [Para 0038]).

Re claim 3, Yoshida teaches the drive device of the light emitting display panel according to claim 1, characterized by being constructed in such a way that in a drive device of the light emitting display panel of a cathode line scan/anode line drive form (See Fig. 1) in which cathodes of the respective light emitting elements are connected to the respective scan lines, the data driver connects the data lines to the scan potential point (Para 0063; "switches are turned on so that the anode drive lines are set to the ground potential.") or sets the data lines in an open state so that a light emitting element of the scan state is controlled not to be lit or to be lit (Para 0019; "to emit light the switch is turned off/open state.").

The limitations of claim 4 are substantially similar to the limitations of claim 3. Therefore it has been analyzed and rejected similar to the rejection of claim 3.

Re claim 18, Yoshida teaches a drive method of a light emitting display panel (1 "display panel" Fig. 1) provided with a plurality of data lines (A1 – An "anode/drive lines" Fig. 1) and a plurality of scan lines (B1 – Bm "cathode/scan lines" Fig. 1) which intersect one another and capacitive light emitting elements (E11 – Enm "Organic EL elements" Fig. 1) having a diode characteristic which are respectively connected, between the data lines and respective scan lines, at intersecting positions between the respective data lines and respective scan lines [See Fig. 2 and Para 0060],

the drive method of the light emitting display panel characterized by performing a reset process in which while the scan lines of the display panel are scanned at predetermined cycles, lighting or non-lighting of the respective light emitting elements of a scan state is controlled in synchronization with the scan and in which all scan lines (Para 0067; "output processing circuit supplies a drive control signal in accordance with the pixel data supplied to the anode line drive circuit in synchronism with the (scan) timing signal/predetermined cycles.)

and all data lines are set at a same electrical potential when the scan is switched so that electrical charges accumulated in parasitic capacitances of the respective light emitting elements are discharged, (Para 0019; "the anode drive line and all cathode scan lines are reset to the ground potential, so that all electric charge is discharged.")

a process which follows this reset process and in which parasitic capacitances of light emitting elements in a non-scan state are charged (Para 0020; "charging is performed by a voltage as shown by arrows for the parasitic capacitance of elements/(non-scanning elements) other than the element that emits light."), utilizing a drive voltage from a driving voltage source, the charge current being supplied to an light emitting element which is scanned and lit as a forward current so that a light emitting element in the display panel is driven to emit light by the charge current, and (As shown by figure 9, the light emitting element E12 is driven by applying the current from the non-scanning elements by utilizing a voltage source Vm along with current source I1 [Para 0020].) and

a process in which all scan lines arranged on the display panel are repeatedly scanned a plural number of times to perform display of one screen (Para 0038; "light-emitting elements in the luminescence display panel are repeated scanned to control light emission/gradation." Fig. 5 shows the change of repeating times of scans. Although, Fig. 5 shows the increase in one line period, over all the changes occur in a unit time of one frame. See Para 0073.) while a repeating times of scans is changeably controlled so that the more the number of repeating times of the scan during a unit time, the higher the entire intensity level becomes and the less the number of repeating times of the scan the lower the entire intensity level becomes (Para 0083; "in a passive matrix display device of this embodiment, when the partial display is selected and the one line period is increased, the light emission time of the display elements is increased/(As can bee seen in Fig. 5, the increase in one line period increases the number of repeating

times of scans), thereby the luminance of a display screen is substantially increased. In addition to the above, since the control is performed so that the ratio of the drive period is increased in the one line period in this embodiment, the luminance of the display screen is substantially further increased.").

Re claim 21, Yoshida teaches the drive device of light emitting display panel according to any one of claims 1 to 4, wherein continuous intensity variable setting is performed by varying an output voltage supplied form the driving voltage source (Para 0072; "the control circuit operates so as to change the cycle of write and read operations for the memory and sends a control signal for changing the output voltage of the variable voltage source in the anode line drive circuit." Also see Para 0083 – 0084).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Abe et al. (Hereinafter "Abe" US 2003/0107542 A1).

Re claim 6, Yoshida teaches the drive device of the light emitting display panel according to any one of claims 1 to 4, characterized by being constructed in such a way that the scan driver is to connect the respective scan lines to the scan potential point and to connect scan lines of the non-scan state which are not connected to the scan potential point to the driving voltage source (See Fig. 9; in 9A, when B1 is scanned, the scan line is connected to a scan potential, and non-scanning lines are connected to a Vm, a voltage source [Para 0019 - 0020].).

But does not explicit disclose the panel characterized by being constructed in such a way that the scan driver is composed of a first scan driver and a second scan driver which are connected to both end portions of respective scan lines, respectively, in the light emitting display panel and that the first scan driver and the second scan driver are in synchronism so as to perform operations.

However, Abe teaches an image display apparatus wherein a first and a second scan drivers are connected to both end portions of scanning lines, and the first and second scan drivers are configured to drive together/in synchronism from the two ends of the panel [Abe: Para 0261].

Therefore, taking the combined teachings of Yoshida and Abe, as a whole, it would have been obvious to a person having ordinary skill in the art to incorporate the

image display apparatus with two scan drivers as taught by Abe to the drive device of light emitting display panel which connects to different scan potentials as taught by Yoshida to obtain a light emitting display panel with two scanning circuits, which connect different scan potentials to scanning and non-scanning lines, thereby decreasing the voltage drop on scanning wires to prevent image quality deterioration [Abe: Para 0261].

4. Claims 8, 10, 12, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view over Corrigan, III (Hereinafter "Corrigan" US 5,559,402).

Re claim 8, Yoshida teaches the drive device of the light emitting display panel according to any one of claims 1 to 4.

But does not explicitly teach a revival means for generating electromotive force, utilizing discharge current of a case where electrical charges accumulated in parasitic capacitances of the respective light emitting elements are discharged is provided and that the electromotive force generated by the revival means is returned to the driving voltage source.

However, Corrigan teaches a driver circuit of an EL device comprising energy recovery/revival means for pumping energy from inductor to a capacitor/(electromotive force) to be used as a driving voltage source by utilizing a discharged current of

electrical charges accumulated in EL elements/parasitic capacitance (Corrigan: Col. 5, lines 29 – 43).

Therefore, taking the combined teachings of Yoshida and Corrigan, as a whole, it would have been obvious to a person of ordinary skill in the art to incorporate the driver circuit of an EL device which could store discharged current as a driving voltage source by using recovery means as taught by Corrigan to the drive device of the light emitting display panel as taught by Yoshida to obtain a drive device of a light emitting device which returns energy/electromotive force generated from discharged current to improve the efficiency of electroluminescent panels and reduce power consumption (Corrigan: Col. 1, lines 40 – 47).

The limitations of claim 10 are substantially similar to the limitations of claim 8. Therefore it has been analyzed and rejected similar to the rejection of claim 8.

Re claim 12, the combined teachings of Yoshida and Corrigan, as a whole, teach the drive device of the light emitting display panel according to claim 8, characterized by being constructed in such a way that an inductor (L2 "Inductor" Fig. 2) which collects the discharge current as electromagnetic energy is provided in the revival means and that electromotive force generated in the inductor (L2 "Inductor" Fig. 2) charges a capacitor arranged in the driving voltage source (Corrigan: Col. 5, lines 29 – 43).

The limitations of claim 14 are substantially similar to the limitations of claim 8. Therefore it has been analyzed and rejected similar to the rejection of claim 8.

The limitations of claim 19 are substantially similar to the limitations of claim 12. Therefore it has been analyzed and rejected similar to the rejection of claim 12.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yong Sim whose telephone number is (571) 270-1189.

The examiner can normally be reached on Monday - Friday (Alternate Fridays off) 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YHS
8/22/2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER